REMARKS/ARGUMENTS

Claims 1-37, 39-44, and 46-48 are pending. Claims 1, 2, 24, 32, and 46 were changed, claims 38 and 45 were cancelled, and claims 47-48 were added by this amendment.

The Examiner rejected claims 1, 24, 32 and 33 under 35 USC §102(b) as being anticipated by Jain et al. The Examiner stated that Jain teaches devices formatting digital bits in a predetermined frame format having no requirement for DC balance by incorporation of the prior art HDLC specification (col. 1, lines 60-68, col. 2, lines 1-2).

Applicant respectfully disagrees, and has amended claims 1, 24, and 32 to clarify these inventions. Claim 1 recites a protocol that comprises digital bits in a predetermined format comprising a frame, where the frame includes digital bits forming a framing cycle and bits forming a data cycle. The framing cycle provides a minimum bit transition frequency allowing clock recovery by the receiving device, and the devices have no requirement for DC balance when formatting the digital bits, where the bits of the frame have an absence of DC balance in their average voltage levels.

Jain does not disclose or suggest a protocol having a frame with a framing cycle providing a minimum bit transition frequency allowing clock recovery, as well as having no requirement for DC balance when formatting the bits and bits having an absence of DC balance in their average voltage levels. The Examiner states that Jain teaches HDLC run length code which is asymmetrical and is DC unbalanced and thus has no requirement for DC balance. However, HDLC coding is *not* used to provide a minimum bit transition frequency allowing clock recovery by a receiving device. HDLC coding "frames" a data packet by surrounding it with framing information like address information, start and stop characters, and error checking data, and may perform bit stuffing to guarantee that the data packet bits do not look like the framing information; there is no provision in HDLC for minimum bit transition frequency for

clock recovery. HDLC coding may be asymmetrical and DC unbalanced by its design and construction, but DC balance is a separate issue from bit transition frequency and clock recovery, and HDLC does not provide a minimum bit transition frequency by its design. Jain does not describe any bus protocol that he is using to provide minimum bit transition frequency for clock recovery. Any such protocol, if present, would exist in addition to the HDLC coding, since HDLC coding does not provide a minimum bit transition frequency for clock recovery. For example, 8B/10B protocol might be used for minimum bit transition in clock recovery in Jain; however, that protocol requires DC balance. Applicant's protocol has no such requirement, thus allowing higher transmission rates and other advantages as described in Applicant's specification.

The Examiner states that Jain discloses a frame forming a framing cycle and a data cycle at col. 2, lines 3-6, and lines 19-23, referenced by the HDLC control symbol and data stream, i.e., framing cycle carrying information relating to the protocol referenced by the HDLC address bits, and a data cycle carrying informational data referenced by HDLC data bits. However, these lines describe the HDLC protocol, which does not provide a minimum bit transition frequency allowing clock recovery by a receiving device. Therefore, the framing cycle of HDLC and Jain does not provide this minimum bit transition frequency as recited in claim 1, and claim 1 is believed patentable over Jain.

Claim 24 recites an improved protocol including a frame cycle and a data cycle, where successive frame cycles provide a minimum bit transition frequency allowing clock recovery by a device receiving the frames. Claim 24 is therefore believed to be patentable over Jain for at least similar reasons as explained above for claim 1. Claims 32 and 33 recite a method of transmitting data according to a protocol, including parsing each frame into bits that form a data cycle and bits that form a frame cycle, where the framing cycles provide a minimum bit transition frequency

allowing clock recovery by a receiving device. Claims 32 and 33 are therefore believed to be patentable over Jain for at least similar reasons as explained above for claim 1.

The Examiner rejected claims 2, 3, 4, 10, 25, 26, 34, 36, and 45 under 35 U.S.C. 103(a) as being unpatentable over Jain in view of Bastiani et al. Claim 45 has been cancelled herein without prejudice. Claims 2, 3, 4, 10, 25, 26, 34, and 36 are dependent on claims 1, 24, and 32, and are believed patentable over Jain for at least the same reasons as explained above. Bastiani does not teach or suggest a framing cycle that provides a minimum bit transition frequency allowing clock recovery by a receiving device as recited in these claims. These claims are therefore believed patentable over Jain in view of Bastiani.

The Examiner rejected claims 5, 6, and 38 under 35 U.S.C. 103(a) as being unpatentable over Jain in view of Bastiani et al. and Derby et al. Claim 38 has been cancelled without prejudice. Claims 5 and 6, which are dependent on claim 1, are patentable over Jain and Bastiani for at least the same reasons as explained above. Derby discloses a frame synchronization pattern for synchronizing frames of data, and teaches or suggests nothing about using a framing cycle to provide a minimum bit transition frequency and clock recovery as recited in Applicant's claim 1. Derby is concerned with synchronizing whole frames of data, not bit transition frequency and clock recovery. Claims 5-6 are therefore believed patentable over Jain in view of Bastiani and Derby.

The Examiner rejected claim 11 under 35 U.S.C. 103(a) as being unpatentable over Jain in view of Bastiani et al. and Bernath. Claim 11 is dependent from claim 1, and Bernath does not teach or suggest a framing cycle that provides a minimum bit transition frequency allowing clock recovery as recited in claim 1, so that claim 11 is believed patentable for at least the same reasons as explained above.

The Examiner rejected claim 46 under 35 U.S.C. 103(a) as being unpatentable over Nickolis in view of Jain. Claim 46 has been amended to clarify that the framing cycle provides a minimum bit transition frequency allowing the receiving circuits to perform clock recovery. The Examiner states that Nickolis discloses at col. 22 lines 62-67 and col. 23 lines 17-31 a common ground and serial bus lines between a processor element array and router I/O element array, enabling the circuits to perform clock recovery as referenced by Table 5 serial-scan clock. The cited table in Nickolis discloses a serial-scan mode that allows serial scan clocking, and a scan clock (SCLK) that is simply a provided clock signal. The Nickolis system does not perform clock recovery from the data stream, but rather a clock is being forwarded in the bus with the data (and uses separate pins). This is a clock forward parallel bus, not a clock recovery bus. Once the clock is forwarded, there is no need for minimum bit transition density in the data to recover the clock, since dedicated pins are used to send the clock on. One disadvantage of a clock forwarding technique like the one in Nickolis is that it does not work at high speeds, as the skew can not be tightly controlled enough across large numbers of pins to enable high frequency.

Thus, there is no disclosure or suggestion in Nickolis about allowing clock recovery by providing minimum bit transition using a framing cycle as recited by claim 46.

In view of the foregoing, Applicant requests that the rejections of claims 1-37, 39-44, and 46 be withdrawn.

Claims 47-48 have been added by this amendment. Claim 47 recites the subject matter of claims 1, 2, and 19, and Claim 48 recites the subject matter of claims 24, 25, and 27. The Examiner stated that these claims would be allowable if rewritten as such. Accordingly, claims 47 and 48 are believed to be patentable over the cited references.

In view of the foregoing, it is submitted that claims 1-37, 39-44, and 46-48 are allowable over the cited references. Accordingly, Applicant respectfully requests reconsideration and passage to issue of claims 1-37, 39-44, and 46-48 as now presented.

Applicant's attorney believes that this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,

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Date

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